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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,214	12/03/2003	Sridharan Ranganathan	42P17693	8008

59796 7590 04/22/2008

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EXAMINER	
WASHINGTON, JAMARES	
ART UNIT	PAPER NUMBER
2625	
MAIL DATE	DELIVERY MODE
04/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,214	RANGANATHAN ET AL.	
	Examiner	Art Unit	
	JAMARES WASHINGTON	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-15,17-25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-15, 17-25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's amendments and response received on March 13, 2008 have been entered. Claims 1-8, 10-15, 17-25 and 27-29 are currently pending in the present application. The amendments and remarks are addressed hereinbelow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5, 13-15 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peter William Mitchell Ilbery (US 20020122210 A1) in view of Venkat V. Easwar et al (US 6781717 B1) and Hoang Nhu (US 5771338).

Regarding claim 1, Ilbery discloses an imaging error diffusion apparatus (Fig. 11 numeral 1100 "apparatus for halftoning") comprising:

a first thread having an error input and a pixel input and producing an error output ("determining the output value of a current pixel using a sum of the input value of the current pixel and a neighborhood error value for the pixel" at paragraph [64]); and

at least one other thread each having a pixel input and an error input, the at least one other thread producing an error output in response to the error output of the first thread ("... adding proportions of the error at the current pixel to the neighborhood error values of yet to be processed pixels of the current and next scanline" at paragraph [66]; shown in Fig. 13);

Ilbery fails to disclose wherein each of the first thread and the at least one other threads execute concurrently.

Easwar et al, in the same field of endeavor teaches a first thread and at least one other thread execute concurrently ("Digital image/graphics processor 71 operates on a three stage pipeline as illustrated in FIG. 4. Data unit 110, address unit 120 and program flow control unit 130 operate simultaneously on different instructions in an instruction pipeline" at Col. 7 lines 39-42; therefore, Easwar et al teaches threads of execution being concurrent).

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the imaging error diffusion apparatus as disclosed by Ilbery et al having a first and at least one additional thread of instruction execution to apply the well known technique of concurrent thread execution as taught by Easwar et al to "reduce overall processing time and thereby maximize throughput" (Col. 4 lines 9-11, Nhu).

Regarding claim 2, Ilbery discloses the apparatus as rejected in claim 1, wherein the at least one other thread is at least two threads (Fig. 13 numerals 1318 and 1320), where each of the other threads has an error input coupled to an error output of another thread (Shown in Fig. 13).

Regarding claim 3, Ilbery discloses the apparatus as rejected in claim 1, wherein the first thread receives error data of a previous row and pixel data of a current row ("In step 1, the total error distributed to a pixel (i,j) from previously processed pixels is referred to as the "neighborhood error" at pixel (i,j)..." at ¶ [178]) and the at least one other thread receives error data of the current row and pixel data of a subsequent row ("...each error sum value in the line store error buffer is associated with a pixel position on the next scanline--a "next scanline pixel"; that error sum value is the sum of error values distributed directly to that next scanline pixel from processed pixels of the current scanline" at ¶ [181]).

Regarding claim 4, Ilbery discloses the apparatus as rejected in claim 1, wherein the apparatus is included within an image signal processor ("The method of Cauchy error diffusion may also be implemented in dedicated hardware such as... digital signal processors" at ¶ [497]).

Regarding claim 5, Ilbery discloses the apparatus as claimed in claim 1, wherein the apparatus is included within a digital media processor ("The method of Cauchy error diffusion may also be implemented in dedicated hardware such as... graphic processors" at ¶ [497]).

Regarding claim 13, Ilbery discloses an imaging error diffusion method comprising:

receiving at a first thread an error input and a pixel input and producing an error output ("... determining the output value of a current pixel using a sum of the input value of the current pixel and a neighborhood error value for the pixel" at ¶ [64]) ; and

receiving at a second thread a pixel input and the error output of the first thread and producing an error output in response to the error output of the first thread

("... adding proportions of the error at the current pixel to the neighborhood error values of yet to be processed pixels of the current and next scanline" at ¶ [66]);

wherein the first thread and the second thread execute concurrently (see rejection of claim 1 wherein the first two threads of execution are utilized).

Regarding claim 14, Ilbery discloses the method as rejected in claim 13, further comprising the first thread calculating an error value for a current pixel based on the pixel input, the error input and at least one other previously calculated error value within the first thread ("... determining an error at the current pixel as the difference between, firstly, the sum of the input value of the current pixel and the neighborhood error value for the pixel, and secondly the output value of the pixel" at ¶ [65]).

Regarding claim 15, Ilbery discloses the method as rejected in claim 13, further comprising receiving at a third thread a pixel input and the error output of the second thread (Shown in Fig. 13 row 1320. Pixel located in the center receiving error results from previous row) and producing an error output in response to the error output of the second thread (Also shown in Fig. 13. Pixel in third row receiving error data from second row and dispersing error

data accordingly based on received data), wherein each of the first thread, the second thread and the third thread execute concurrently (see rejection of claim 1).

Regarding claim 20, Ilbery discloses a system comprising

a memory (Fig. 21 numeral 2106 "memory"); and

a processor coupled to the memory (Fig. 21 numeral 2105 "processor" coupled to memory by bus line 2104); and

an imaging error diffusion apparatus (Fig. 11 numeral 1100 "apparatus for halftoning") comprising:

a first thread having an error input and a pixel input and producing an error output ("determining the output value of a current pixel using a sum of the input value of the current pixel and a neighborhood error value for the pixel" at ¶ [64]); and

at least one other thread each having a pixel input and an error input, the at least one other thread producing an error output in response to the error output of the first thread ("... adding proportions of the error at the current pixel to the neighborhood error values of yet to be processed pixels of the current and next scanline" at ¶ [66]. Shown in Fig. 13), wherein each of the first thread and the at least one other threads execute concurrently (see rejection of claim 1).

Regarding claim 21, Ilbery discloses the system as rejected in claim 20, wherein the error output of the first thread is not stored in memory (Fig. 9. The error output for each "current" pixel is "held" in line error buffer 930 until outputted to line 928. The output is not "stored" in memory. ¶ [170]).

Regarding claim 22, Ilbery discloses the system as rejected in claim 20, wherein the error output of the first thread is not stored in any memory external to the threads (Fig. 9 shows error diffusion processing per pixel. Error output is held in a line error buffer "numeral 930"... ¶ [170]).

2. Claims 6-8 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilbery, Easwar and Nhu as applied to claims 1 and 20, and further in view of Michael Webb et al (US 5553165 A).

Regarding claim 6, Ilbery discloses the apparatus as rejected in claim 1 above.

Ilbery fails to disclose or suggest a total number of the first thread and the at least one other threads is equal to or greater than a number of stages in an error diffusion hardware pipeline.

Easwar teaches, in the same field of endeavor of digital image/graphics processing discloses a well-known operation for a processor implementing a three stage pipeline ("Digital image/graphics processor 71 operates on a three stage pipeline as illustrated in FIG. 4. Data unit 110, address unit 120 and program flow control unit 130 operate simultaneously on different instructions in an instruction pipeline. The three stages in chronological order are fetch, address and execute. Thus at any time, digital image/graphics processor 71 will be operating on differing functions of three instructions" at Col. 7 line 39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an image processor as taught by Easwar where the processing is performed in three stages to the imaging error diffusion apparatus of Ilbery to allow the error diffusion processing of Ilbery to operate on differing functions of three instructions to speed processing of multiple threads. One thread does not have to wait for the previous thread to perform all processing before execution begins.

Ilbery and Easwar teach a three stage error diffusion processing pipeline as described above.

Ilbery and Easwar fail to teach or suggest a total number of the first thread and the at least one other threads being equal to or greater than the number of processing stages in the error diffusion pipeline.

Webb teaches, in the same field of endeavor of parallel error diffusion methods, a first thread (Fig. 8 numeral 42) and the at least one other threads (Fig. 8 numerals 43 and 44 with numeral 45 starting a new thread of processing from the first line of execution (numeral 42) as described "In a further embodiment, depicted in FIG. 8, further parallelization of the error diffusion process is achieved by error diffusion processes 42, 43, 44 error diffusing the current input screen. When the error diffusion process 42 finishes with its current line, it will immediately begin on the next line 45 requiring error diffusion" at paragraph 5 line 61) is equal to or greater than a number of stages in an error diffusion hardware pipeline (Three processing threads as taught by Webb equaling three processing stages as taught by Easwar above.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Webb where three threads simultaneously execute

multiple stages of error diffusion processing as disclosed in the apparatus of the Ilbery-Easwar combination because it would "[allow] the error diffusion process to be carried out in parallel while still being able to keep up with a high input data rate which may be required" (at paragraph 6 line 13, Webb).

Regarding claim 7, Ilbery discloses the apparatus as rejected in claim 6, wherein the total number of the first thread and the at least one other threads is equal to the number of stages in the error diffusion hardware pipeline (see rejection of claim 6 above).

Regarding claim 8, Ilbery discloses the apparatus as claimed in claim 7, wherein the total number of the threads and the number of the stages is three (see rejection for claim 7 above).

Regarding claim 23, Ilbery discloses the system as rejected in claim 20, wherein a total number of the first thread and the at least one other threads is equal to or greater than a number of stages in an error diffusion hardware pipeline included in the processor as rejected in claim 6 above.

Regarding claim 24, Ilbery discloses the system as claimed in claim 23, wherein the total number of the first thread and the at least one other threads is equal to the number of stages in the error diffusion hardware pipeline as rejected in claim 7 above.

Regarding claim 25, Ilbery discloses the apparatus as claimed in claim 24, wherein the total number of the threads and the number of the stages is three as rejected in claim 8 above.

3. Claims 10-12, 17-19 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ilbery, Easwar and Nhu as applied to claims 1, 13, and 20 above, and further in view of Jae Hyuck Lee (US 6956583 B2).

Regarding claim 10, Ilbery discloses the apparatus as rejected in claim 1 above.

Ilbery fails to teach the method performed by the apparatus wherein the first thread has a second error input.

However, Lee, in the same field of endeavor, teaches the first thread having a second error input ("... a gray-level is implemented by multiplying a coefficient by an error value between three pixels placed the upper horizontal line and a left pixel centering around a present pixel and adding an error value of the present pixel in accordance with a carry occurrence" at paragraph 1 line 34. This method teaches the current pixel using an error generated by surrounding pixels and an error of the present pixel which would constitute two error input values.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Lee where two error inputs are used as the input error for the method performed by the apparatus of Ilbery as disclosed above in claim 1 because one would obtain a more accurate error result.

Regarding claim 11, Ilbery discloses the apparatus as rejected in claim 10 above, wherein each of the at least one other threads has a second error input. Using the above method, each pixel is processed by the same algorithm.

Regarding claim 12, Ilbery discloses the apparatus as rejected in claim 1, wherein each of the at least one other threads has a second error input. (See rejection of claim 10 above).

Regarding claim 17, Ilbery discloses the method of claim 13, wherein the first thread receives a second error input as rejected in claim 10 above.

Regarding claim 18, Ilbery discloses the method of claim 17, wherein the second thread receives a second error input as rejected in claim 11 above.

Regarding claim 19, Ilbery discloses the method of claim 13, wherein the second thread receives a second error input as rejected in claim 12 above.

Regarding claim 27, Ilbery discloses the system as claimed in claim 20, wherein the first thread has a second error input as rejected in claim 10 above.

Regarding claim 28, Ilbery discloses the system as claimed in claim 27, wherein each of the at least one other threads has a second error input as rejected in claim 11 above.

Regarding claim 29, Ilbery discloses the apparatus as claimed in claim 20, wherein each of the at least one other threads has a second error input as rejected in claim 12 above.

Response to Arguments

4. Applicant's arguments received March 13, 2008 have been fully considered but they are not persuasive.

Applicant's remarks: None of the cited references relied upon by the Examiner teaches or even suggests that the threads execute concurrently. The examiner has made a sweeping statement that this feature is included Ilbery, Easwar or Webb without particularly pointing out how or where such feature is taught by any of these references either alone or in any possible combination thereof.

Examiner's response: Easwar et al clearly explains, at Col. 7 lines 39-42, instructions concurrently being executed in a three stage pipeline. This method of processing is thus well-known in the art and would have been obvious to combine the teachings with the error diffusion processing of Ilbery as rejected in claim 1.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMARES WASHINGTON whose telephone number is (571)270-1585. The examiner can normally be reached on Monday thru Friday: 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Poon can be reached on (571) 272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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April 15, 2008